

Temperature Effects on MOSFET-Like Carbon Nanotube Field Effect Transistors

Mostafa Fedawy, Wael Fikry, Adel Alhenawy, Hazem Hassan

Abstract— The Carbon Nanotube Field Effect Transistor (CNTFET) can be considered as one of the promising new transistors because it can avoid most of traditional Metal Oxide Semiconductor Field Effect Transistor (MOSFET) limitations. In this work we present the influence of temperature on the transfer and output characteristics of the MOSFET-Like Single-Walled Carbon Nanotube Field Effect Transistor (SWCNTFET). The simulation results are performed using our four-subband model which is valid for high and low gate voltage, up to 2 V. Our results prove that the higher subbands have a drastically effect on the saturation drain current especially for high gate voltage. On the other hand, we clarify that the sub-threshold region characteristics are depended only on the first subband. Furthermore, we study the onset-voltage, the on-/off-current ratio, and the sub-threshold swing of the SW-CNTFETs. Results show that, the onset-voltage is decreased linearly with increasing the temperature. Moreover, the rate of change in the onset-voltage with temperature is almost independent on the drain voltage. Unlike the silicon based transistor, both the on- and off-current are increased as the temperature increased. In addition, we show that the on-/off-current ratio will be reduced dramatically when the temperature increased from T=100 K to T=300 K. Moreover, results show that the sub-threshold swing is increased linearly with increasing the temperature and it is almost independent on the drain-source voltage.

Index Terms— CNTFET characteristics, four-subband model, MOSFET-Like SW-CNTFET, SW-CNTFET, temperature effects.

1 INTRODUCTION

THE MOSFET devices will be reaching to its limits in 2020 when the channel length of MOSFET is below 10nm. For this reason, researchers are looking for different materials and devices replace the silicon-based field effect transistor [1]. Some novel nanoelectronic devices have been suggested to replace the MOSFET such as CNFETs, Single Electron Transistors (SETs) and resonant tunnelling devices [2]-[3].

Among the devices suggested, CNTFET appears as one of the promising alternative devices because of both their semi-conducting properties and their ability to carry high current. Carbon nanotubes are two dimensional graphene sheet rolled into cylindrical shape with diameter in nanometres scale. The orientation in which the CNTs are rolled (chirality) can make them behave like metallic or semi-conducting material.

Like the MOSFETs, the CNTFETs are three terminals device. The main difference is that CNTFETs employ the CNT as a channel between the source and the drain terminals whereas MOSFETs channel is made of doped silicon. According to the number of layer that used in the channel device, the CNTFETs can be Single Wall (SW) or Multi Wall (MW). CNTFETs have two modes of operation, the Schottky Barrier (SB) or MOSFET-Like CNTFETs. In the SB-CNTFETs the gate voltage modulates the current which flow in the channel by changing the width of the barrier. But in MOSFET-Like CNTFETs the gate voltage can be controlled in the drain current by changing the height of the barrier. In this work, we treat with MOSFET-Like

SW-CNTFETs [4]-[5].

There are varies numerical models concerned with only the first subband current in order to investigate the performance and the behaviour of CNTFET [6], [7], [8], [9]. In the latest our work, we proposed an accurate model valid for low and high gate voltage taking into account the higher subbands [10], [11], [12]. In the present work, we used this model to study the effect of temperature on the transfer characteristics curves of MOSFET-Like SW-CNTFETs. Moreover, the influence of temperature on sub-threshold swing, on-state current, and off-leakage current are investigated.

2 CNTFETS SIMULATION MODEL

Generally, the total carrier density and the drain current in CNTFETs are dependent on the number of effective subbands which calculated from the subband minima (Δ). We used the tight binding method to construct the graphene band structure. Then we use the zone folding method to calculate the all subband minima accurately [12]. Thus the induced carrier density (ΔN) can be given by.

$$\Delta N = g_0 \sum_p \int_0^\infty [N_{1p}(z) + N_{2p}(z)] dz - N_e \quad (1)$$

Where

$$N_{1p}(z) = \frac{1}{1 + \exp \left[\frac{\sqrt{z^2 + \Delta_p^2} + (\Delta_{f1} - \Delta_p)}{K_B T} \right]} \quad (2)$$

- Mostafa Fedawy is PHD candidate in Ain Shams University, Cairo, Egypt. Mustafa.Fdawwy@staff.aast.edu
- Wael Fikry is lecturer in Umm Al Qura University, Makkah, KSA. wael_fikry@ieee.org
- Adel Alhenawy is lecturer in Ain Shams University, Cairo, Egypt. a.henawy@hotmail.com
- HAZEM Hassan is lecturer in AASTMT University, Cairo, Egypt. HAzem@aast.edu

$$N_{2p}(z) = \frac{1}{1 + \exp\left[\frac{\sqrt{Z^2 + \Delta_p^2} + (\Delta_{f2} - \Delta_p)}{K_B T}\right]} \quad (3)$$

Where Z is given by (4), $y = (E - E_{Cp})$, g_0 is the metallic density of states, p is the number of effective subbands, Δ_p is the p^{th} subband minima, T is the temperature in Kelvin, and Δ_{f1} and Δ_{f2} are given by (5) and (6) respectively

$$Z = \sqrt{(E - E_{Cp} + \Delta_p)^2 + \Delta_p^2} \quad (4)$$

$$\Delta_{f1} = E_{Cp} - E_{f1} - U_{SCF} \quad (5)$$

$$\Delta_{f2} = E_{Cp} - E_{f2} - U_{SCF} \quad (6)$$

Where E_{f1} and E_{f2} is the source and drain Fermi level respectively, E_{Cp} is the conduction band edge for the p^{th} subband and U_{SCF} is the self-consistent potential, given by [4]-[6].

$$U_{SCF} = \left[U_L + \frac{q^2 \Delta N}{C_\Sigma} \right] \quad (7)$$

Where U_L and C_Σ are the Laplace potential and the total channel capacitance respectively.

Furthermore, the drain current (I_D) from all subbands can be given by

$$I_D = \frac{2qK_B T}{h} \sum_p \int_0^\infty [I_{1p}(y) + I_{2p}(y)] dy \quad (8)$$

Where

$$I_{1p}(y) = \frac{1}{1 + \exp\left[\frac{y + \Delta_{f1}}{K_B T}\right]} \quad (9)$$

$$I_{2p}(y) = \frac{1}{1 + \exp\left[\frac{y + \Delta_{f2}}{K_B T}\right]} \quad (10)$$

Equation (1) and (8) show that the number of subbands has a drastically effect on the drain current calculations. It is also obvious that the total induced carrier and the total drain current are strongly dependent on the operating temperature and the channel potential. In the following section we will investigate the effect of the temperature in saturation and sub-threshold regions.

3 RESULTS AND DISCUSSION

In this section, we study the temperature effects on the CNT-FETs' characteristics as well as the influence of number of subbands in the drain current calculations. For all simulations, we take CNT chiral vector equal to $m = 26$, $n = 0$ which is consider as the most common used chirality [4]-[5]. Furthermore,

we neglect the change in the subband minima due to the temperatures variation. The reason is that when the temperature changed from 0 to 400 K, the variation in the subband minima is less than 0.006 eV which is neglected value [13].

Fig. 1 shows the output characteristics of MOSFET-like SW-CNTFETs for different values of applied gate voltage at temperature 300 and 500 K using one- and four-subband model. The four-subband model means that the first four subbands are used in order to calculate the drain current. It is evident that as the gate voltage increased the amount of the change in the saturation drain current between the two models is increased. The reason is that, at low gate voltage, the channel energy levels are shifted down slightly therefore the first subband has a dominant effect in the drain current calculation. However, for high gate voltage, more channel levels are pushed down therefore more subbands will be participated in the drain current calculation and consequently the saturation drain current will be increased. For instance, at $V_{ds} = V_{gs} = 0.6$ V, the four-subband model presents a drain current higher than that presented by the one-subband model with 25.6 %. Moreover, When the gate voltage increased to 1 V, this percentage will be increased to 42.2 % at $V_{ds} = 0.6$ V. Unlike the MOSFET, when the four-subband model is used, it is evident that the saturation drain current of SW-CNTFET is increased with increasing the temperature. The reason is that, in MOSFETs, the temperature dependency of the saturation drain current originates from the carriers mobility which is decreased with increasing the temperature. However, in SW-CNTFETs the dependency mainly originates from the expansion that occurs in the Fermi function with increasing the temperature. Therefore, the number of available states which are contributed from all subbands will be increased. Consequently, the saturation drain current will be increased. This behaviour does not appear clearly if the one-subband model is used because of the expansion that occurs in the Fermi function has a slightly effect in the first subband.

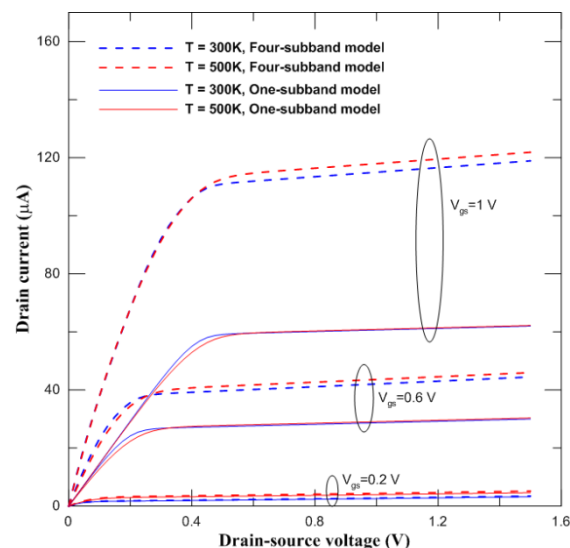


Fig. 1. The output characteristics of SW-CNTFET using one- and four subband model at temperature 300 and 500 K.

Fig. 2 depicts the influence of temperatures on the transfer characteristics of MOSFET-Like SW-CNTFETs at $V_{ds} = 100$ mV using one- and four-subband model. For both models, in the sub-threshold region, it is clear that the drain current will be increased with increasing the temperature. The reason is that when the temperature increased, the source-channel barrier is decreased and then the number of transferred carriers from the source to the channel will be increased. Generally, the sub-threshold slope is a feature of the transistors' transfer characteristic and it can be calculated by reciprocating the sub-threshold swing. From Fig. 2, it is clear that the slope of the drain current at $T = 300$ K is higher than that at $T = 500$ K where the sub-threshold swing is approximately 66 mV/decade and 126 mV/decade at temperature 300 and 500 K, respectively. Moreover, it is evident that, the sub-threshold regions of one- and four-subband model are coincident at the same value of temperature. This result indicates that the drain current in the sub-threshold region is depended only on the first subband. From the perspective of circuit designer, it is important to know the gate voltage at which the sub-threshold region departs from its linearity in the logarithmic scale (which is corresponding to threshold voltage in the MOSFET model). In this work, we named the amount of this gate voltage as the onset-voltage. Our result shows that the onset-voltage is independent on the number of the subbands that used in the model. Thus, we can conclude that the first subband is the only subband which responsible for sub-threshold region.

Fig. 3 shows the influence of temperature on the onset-voltage at $V_{ds} = 100$ mV and 1V. It is clearly observed that, the onset-voltage is decreased almost linearly as the temperature increased. We can notice that, the rate of change in the onset-voltage with temperature is almost independent on the drain voltage. Moreover, Fig. 3 depicts the dependency of the onset-voltage on the drain voltage. This phenomenon likes the Drain Induced Barrier Lowering (DIBL) effect in the MOSFET.

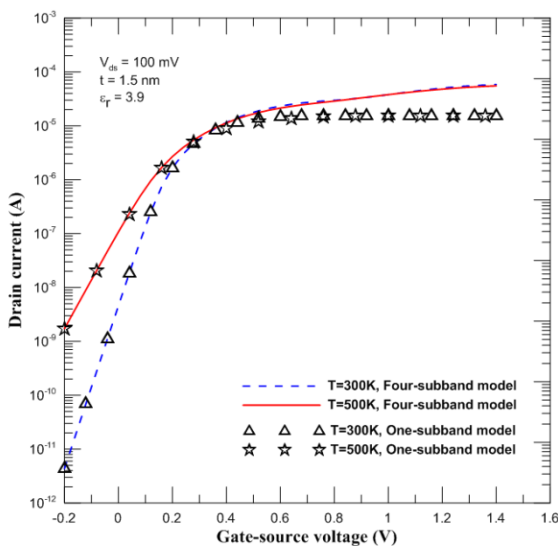


Fig. 2. The transfer characteristics of SW-CNTFET using one- and four-subband model at temperature 300 and 500 K.

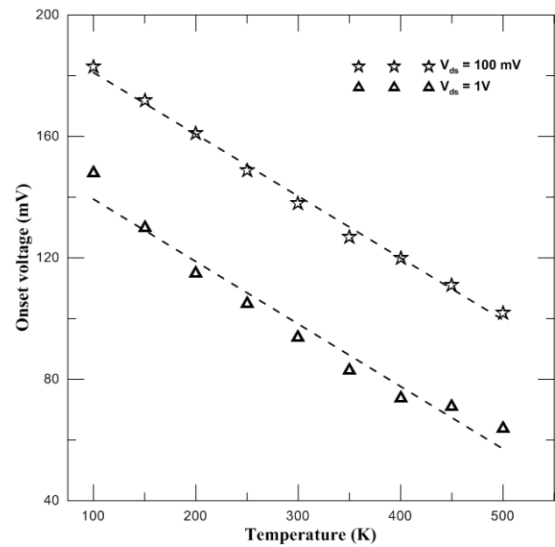


Fig. 3. The variation of the onset-voltage with temperature at $V_{ds} = 0.1$ and 1V.

The off-leakage current (I_{OFF}) and the on-state current (I_{ON}) are one of the most important parameters in the circuit design. The off-leakage current is the drain current at $V_{gs} = 0$ whereas the on-state current (I_{ON}) is the drain current at $V_{gs} = V_{ds}$. Fig. 4 illustrate the off-leakage and the on-state currents versus the temperature at $V_{ds} = 100$ mV, using the four-subband model. Like the conventional MOSFET, it is clear that, the off-leakage current is increased as the temperature increased. It is also obvious that, at high temperature, the leakage current will be very high and then the gate voltage will lose its control on the channel. Unlike the conventional MOSFET, Fig.4 confirmed that the on-state current is increased with increasing the temperature.

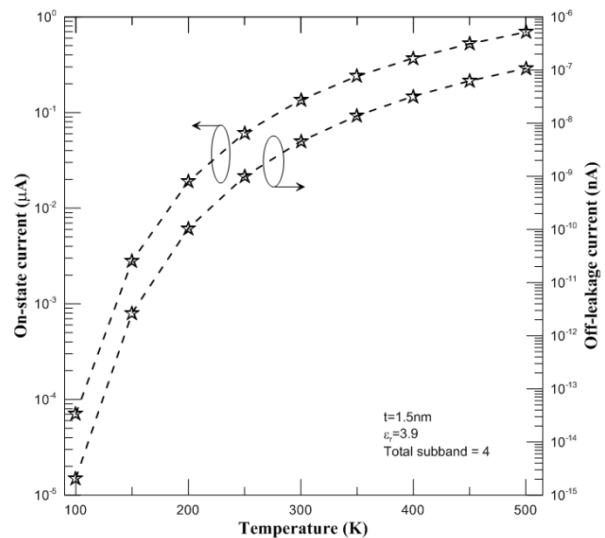


Fig. 4. The off-leakage current ($V_{gs} = 0$) and the on-state current ($V_{gs} = V_{ds}$) versus the temperature.

As well known, the on-/off-current ratio is very important to the circuit designers. Fig. 5 illustrates the on-/off-current ratio versus the temperature for low and high drain-source voltage. It is clear that by increasing the temperature the on-/off-current ratio is decreased. For low drain voltage, at $V_{ds} = 100$ mV, we can notice that when the temperature changed from 100 to 300 K, the on-/off-current ratio is reduced approximately with three order of magnitude. Therefore, the off-leakage current is more influenced with the temperature spatially from $T = 100$ to 300 K whereas the increment in the off-current is comparable with the on-state current from $T = 300$ till 500 K.

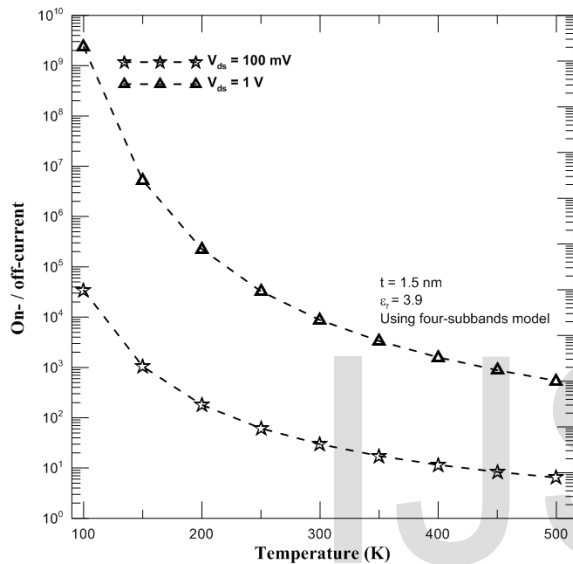


Fig. 5. On-/off-current ratio versus the temperature at $V_{ds} = 100$ mV and 1V.

The sub-threshold swing is very important parameter where it displays the steepness of the switching response. Using the four-subband model, the sub-threshold swing versus the temperature for low and high drain voltage is shown in Fig. 6. It is clear that the sub-threshold swing is slightly affected with the drain voltage. Moreover, for low and high drain-source voltage, the temperature has considerable effect on the sub-threshold swing. It is obvious that the sub-threshold swing will be increased with increasing the temperature. At $V_{ds} = 1$ and 0.1 V, the sub-threshold swing will be increased approximately by 69 % when the temperature changed from 100 to 500 K. It also can be seen that the sub-threshold swing is increased linearly with slope = 0.22 mV/K when the temperature increased.

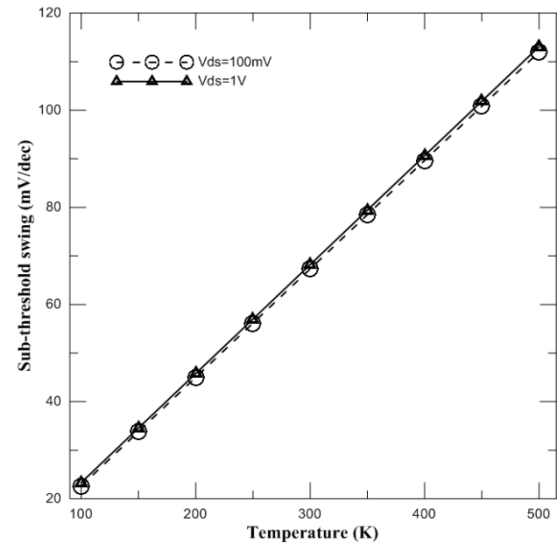


Fig. 6. The effect of temperature on the sub-threshold swing at $V_{ds} = 100$ mV and 1 V.

4 CONCLUSION

In this paper, we have investigated the effects of the temperature on the output and transfer characteristic of MOSFET-Like SW-CNTFETs. Our results show that the number of contributed subbands has a great effect in the drain current calculation. Moreover, the saturation drain current is increased by 42 % at $V_{ds} = 0.6$ V and $V_{gs} = 1$ V when we use the four-subband model instead of one-subband model. Furthermore, we explain the effect of temperature on the onset-voltage where it is decreased with slope = 0.5 mV/K with increasing the temperature. Also, we observed that the sub-threshold swing is increased by 0.22 mV/K even at high or low drain-source voltage.

REFERENCES

- [1] K. Roy, S. Mukhopadhyay, and H. Mahmoodi-Meimand, "Leakage current mechanisms and leakage reduction techniques in deep-submicrometer CMOS circuits," *Proceedings of the IEEE*, vol. 91, no. 2, pp 305-327, February 2003
- [2] Neil M. Zimmerman, William H. Huber, Akira Fujiwara, and Yasuo Takahashi, "Excellent charge offset stability in a Si-based single-electron tunneling transistor", *Applied Physics Letters*, vol 79, no. 19, pp 3188- 3190, 2001
- [3] Wu, K. Y., I. S. Yu, K. Y. Wang, H. H. Cheng, K. M. Hung, G. Sun, and R. A. Soref. "Si-based resonant tunneling diodes for room temperature operation," In *Nanoelectronics Conference(INEC)*, 2010 3rd International, Hongkong, pp. 1252-1253. IEEE, 2010.
- [4] S. Datta, *Quantum transport - Atom to transistor*, Cambridge University Press, Shaftesbury Road, Cambridge, CB2 2RU, 2005, ch. 1.
- [5] J. Guo and M. Lundstrom, *Nanoscale Transistors: Device Physics, Modeling and simulation*. New York: Springer-Verlag, 2006, ch. 5.
- [6] Arijit Raychowdhury, Ali Keshavarzi, Juanita Kurtin, Vivek De, and Kaushik Roy, "Carbon nanotube field-effect transistors for high-performance digital circuits— DC analysis and modeling toward optimum transistor structure," *IEEE Trans. Electron Devices*, vol. 53, no. 11, pp. 2711-2717, Nov. 2006.
- [7] Thao Dang, Lorena Anghel, and Regis Leveugle, "CNTFET Basics and Simulation," *International Conference on Design and Test of Integrated Systems in Nanoscale Technology*, DTIS 2006, pp. 28-33, IEEE, 2006.

- [8] Subhajit Das, Sandip Bhattacharya, and Debaprasad Das, "Design of Digital Logic Circuits using Carbon Nanotube Field Effect Transistors", *International Journal of Soft Computing and Engineering*, vol. 1, no. 6, pp. 173-178, Dec. 2011.
- [9] Robert Seidal, Andrew P. Graham, Eugen Unger, Georg S. Duesberg, Maik Liebau, Werner Steinhögl, Franz Kreupl, Wolfgang Hoenlein, and Wolfgang Pompe, "High-current nanotube transistors," *Nano Letters*, vol. 4, no. 5, pp. 831-834, 2004.
- [10] Ali Javey, Ryan Tu, Damon B. Farmer, Jing Guo, Roy G. Gordon, and Hongjie Dai, "High performance n-type carbon nanotube field-effect transistors with chemically doped contacts," *Nano Letters*, vol. 5, no. 2, pp. 345-348, 2005.
- [11] Kenji Natori, Yoji Kimura, and Tomo Shimizu, "Characteristics of a carbon nanotube field-effect transistor analyzed as a ballistic nanowire field-effect transistor," *J. Appl. Phys.*, vol. 97, no. 3, pp. 034306.1-034306.7, 2005.
- [12] M. Fedawy, W. Fikry, A. Alhenawy, H. Hassan, "I-V Characteristics Model for ballistic Single Wall Carbon Nanotube Field Effect Transistors (SW-CNTFET)" 2012 IEEE Int. Conf. on Electronics Design, Systems and Applications, Kuala Lumpur, pp. 10-13.
- [13] Rodrigo B. Capaz, Catalin D. Spataru, Paul Tangney, Marvin L. Cohen, Steven G. Louie, "Temperature Dependence of the Band Gap of Semiconducting Carbon Nanotubes," *Phys. Rev. Lett.* vol. 94, no. 3, pp. 036801.1- 036801.4, 2005.

IJSER